UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/353,547	07/14/1999	STEFANOS SIDIROPOULOS	9797-022-999	3752

24341	7590	11/19/2003

Pennie & Edmonds, LLP
3300 Hillview Avenue
Palo Alto, CA 94304

EXAMINER
KIM, KEVIN

ART UNIT	PAPER NUMBER
2634	8

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _22 August 2003_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-7,9-73_ is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _1-7,9,10,20,31-34 and 50-73_ is/are allowed.

6)☒ Claim(s) _11,12,15,16,18,19,21,24-29,35,37,40-45,47 and 49_ is/are rejected.

7)☒ Claim(s) _13,14,17,22,23,30,36,38,39,46 and 48_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

　　a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.

4) ☐ Interview Summary (PTO-413) Paper No(s). _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments with respect to the rejected claims have been considered

but are moot in view of the new ground(s) of rejection.

2.   The text of those sections of Title 35, U.S. Code not included in this action can be

found in a prior Office action.

Claim Rejections - 35 USC § 102

3.   Claims 11,12 are rejected under 35 U.S.C. 102(e) as being anticipated by Woeste

et al. (US 6,232,806 cited previously)

Referring to Figs. 1A and 1B, Woeste et al discloses assessing a plurality of phase

delays (54,64) between a master device (22) and slave modules (34,44), identifying a

selected phase delay for a selected slave device, see variable delay lines associated with

respective slave devices, and transmitting data based on the selected phase delay.

Regarding claim 12, in order to identify a selected phase delay a corresponding

slave device is first designated.

Claim Rejections – 35 USC § 103

4.   Claims 15,16,18,19,21,24-29,35,37,40-45,47 and 49 are rejected under 35 U.S.C.

103(a) as being unpatentable over Woeste et al (US 6,232,806 cited previously) in view

of Ueda (US 5,889,824).

Consider claim 15. Woeste et al discloses a plurality of slave devices having no

phase alignment circuitry, see Fig.1B, and a master device (22) with "a universal phase

alignment circuitry." The master device stores a plurality of phase values for the

plurality of slave devices (56,66) for synchronous communication with the slave devices.

Woeste fails to teach "an addressable register bank" to store the phase values. Referring

to Fig.2, Ueda teaches a memory (23), i.e., "an addressable register bank," for storing and

retrieving phase differences between a reference and a received clock signal so that it

appears that the exact adjustment to the clock signal can be performed given a phase

difference. See col. 4, line 56- col.5, line 9. Thus, it would have been obvious to one

skilled in the art at the time the invention was made to store the phase offset in a memory

in the master/slave synchronization method of Woeste et al, as taught by Ueda for the

purpose of providing a predetermined amount of phase delay corresponding to the phase

offset.

Regarding claim 16, "a first selected phase value" such as determined by the

control logic (56) is used to alter a system clock, see variable line delay (52) for example,

to establish a master device receive data clock signal to receive data from the selected

slave device (34).

Regarding claim 18, the phase detector of the master device performs "a

calibration operation" to identify the phase values.

Regarding claim 19, the detected phase offsets are added to the respective

variable line delays.

Consider claims 21, 27,37 and 43. Referring to Fig.1A, Woeste et al discloses a

"method of calibrating transmission of data from a master device to a first slave device,"

by putting the master and the slave devices in an in-phase relationship. The method

comprises determining a phase offset from the master device to the slave device. See

Phase Detectors 54, 56 and col.6, lines 40-44. The phase offset is stored in the control

logic (134) of the master. See col.8, lines 17-21. The stored phase offset is used in the transmission of data from the master to the slave device. Woeste fails to teach the use of "an addressable register bank" to store the phase offset. Referring to Fig.2, Ueda teaches a memory (23), i.e., "an addressable register bank," for storing and retrieving phase differences between a reference and a received clock signal so that it appears that the exact adjustment to the clock signal can be performed given a phase difference. See col. 4, line 56- col.5, line 9. Thus, it would have been obvious to one skilled in the art at the time the invention was made to store the phase offset in a memory in the master/slave synchronization method of Woeste et al, as taught by Ueda for the purpose of providing a predetermined amount of phase delay corresponding to the phase offset.

Regarding claims 24,40 see the "data" is transmitted from the master to the slave device. See the path B from the master to the slave device.

Regarding claims 25, 28,41,44 the path B reads on "a request line" while the path A reads on as "a data line." See Fig.1A and 1B.

Regarding claims 26,42, see data is transmitted from the slave to the master along the transmission path A.

Regarding claims 29, 45, Fig.3A shows phase offset values being determined and stored for each of the salve devices.

Regarding claims 35 and 47 Woeste et al discloses all the subject matter claimed except for using the offset value in the transmission of data over a plurality of data/request lines. However, it is well known in the art two communication device could communicate over a plurality of data lines such as parallel data communication. Thus, it would have been obvious to one skilled in the art at the time the invention was made to

provide a plurality of data lines between the master device and the slave device for

parallel communication, in which case all the lines would be equally phase adjusted

based on the determined phase offset between the master device and the slave device.

Regarding claim 49, since the signal transmitted from the master to the slave is

to determine phase offset, the content of the signal is immaterial and thus it would have

been obvious to carry any information including a portion of an access request.

Allowable Subject Matter

5. Claims 1-7,9,10, 20,31-34,50-73 allowed.

6. Claims 13,14, 17,22,23,30, 36,38, 39,46,48 are objected to as being dependent

upon a rejected base claim, but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should

be directed to Kevin Y Kim whose telephone number is 703-305-4082. The examiner can normally be

reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this

application or proceeding is assigned is 703-872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be

directed to the receptionist whose telephone number is 703-305-3900.

kvk

STEPHEN CHIN
SUPERVISORY PATENT EXAMINE:
TECHNOLOGY CENTER 2600